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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RODRIGUEZ, GLENDA P	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,009	HEYDARI ET AL.	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30, 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30, 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Patapoutian et al. (US Patent No. 5, 661, 760).

Regarding Claims 1, 4, 8, 20, 24, 27, 32 and 33, Patapoutian et al. teaches a coded binary sequence, which has a first group bits that are consecutive, the first group having first and second separate portions both representing a first state, the bits in the first portion having a second logic level and the bits in the second state having a third logic level (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary 1s into "--++" and binary zeros into "++--", each having two differing states. It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).); and a second group of consecutive bits each having the same state, the second group representing a second logic level (See Col. 4, L. 43-44, wherein "--++++--", which are four consecutive symbols having the same state).

Claim 10 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 10 however also recites the following limitations: "disk sectors operable to store application data and servo wedges that store servo data" (Pat. No. 5, 661, 760; Col. 6, Lines 15-61 and Col. 6, Lines 15-61).

Claim 11 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 11 however also recites the following limitations: "a Viterbi detector" (Pat. No. 5, 661, 760; See Abstract).

Claim 14 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: "a sample circuit to generate samples of a signal" (Pat. No. 5, 661, 760; See Abstract).

Claim 16 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: "a data storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data, a motor, a read head and a read head positioning circuit and a servo circuit" (Pat. No. 5, 661, 760; Col. 5, Lines 15-21 and Col. 6, Lines 15-61, Servo data are used for non-application purposes).

Regarding Claim 2, Patapoutian et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second portions of the first group respectively comprise first and second halves of the first group (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that the first group with two portions (group "10") can be divided in to first and second halves: "10" or "--++++--" can be divided into "--++" and "++--".).

Regarding Claim 6, Patapoutian et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second groups each respectively comprise four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 7, Patapoutian et al. and teach all the limitations of Claim 4. Patapoutian et al. further teach the first and second portions of the second group respectively comprises first and second halves of the second group ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claim 12, Patapoutian et al. teach all the limitations of Claim 11. Patapoutian et al. further teaches wherein the binary sequence comprises a coded binary sequence (See Abstract).

Regarding Claim 13, Patapoutian et al. teach all the limitations of Claim 11. Patapoutian et al. further teach wherein the first logic level comprises a logic 0; and the second logic level comprises a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "10" will be encoded into "--++++--", having a first and second equally sized portion in the first group ("--++" and "++--").).

Regarding Claim 15, Patapoutian et al. teach all the limitations of Claim 14. Patapoutian et al. further teach a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence (Col. 11, Lines 3-25 and Lines 57-62).

Regarding Claim 17, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal (See Abstract); and a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal (Col. 5, Line 64 to Col. 6, Line 13 and Abstract and Fig. 1).

Regarding Claim 18, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises a decoder operable to decode the recovered servo data (See Abstract. Patapoutian et al. teaches that the Viterbi detector also decodes the ¼ signal.).

Regarding Claim 19, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teach wherein the read head comprises a read-write head (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63 and Col. 12, Lines 1-12).

Regarding Claims 3, 5, 9, 21 and 34, Patapoutian et al. teach all the limitations of Claims 1, 4, 8, 20 and 34, respectively. Patapoutian et al. further teach wherein the first, second, third, and fifth logic levels respectively equal a logic 1 and a logic 0; the first and second logic states respectively equal 0 and logic 1; and the same state equals a logic 0 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 22, Patapoutian et al. teach al the limitations of Claim 20. Patapoutian et al. further teaches wherein the coding comprises: coding the first logic level as a first group of four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive

bits (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--"); and coding the second logic level as a second group of four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 23, Patapoutian et al. teach all the limitations of Claim 20. Patapoutian et al. further teach wherein the first and second portions of the first group respectively comprise first and second halves of the first group ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 28, Patapoutian et al. teach all the limitations of Claim 27. Patapoutian et al. further teaches wherein: the first and second code symbols each comprise a number of code bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Col. 3, Lines 55-58). Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").); and the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claims 25, 26 and 29, Patapoutian et al. teach all the limitations of Claims 24 and 27, respectively. Patapoutian et al. further teach wherein: the first logical bit equals a logic 0; and the second logical bit equals a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent

that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 30, Patapoutian et al. teach all the limitations of Claim 27. Patapoutian et al. further teaches wherein each of the first and second groups of code words is or is approximately half as long as the first code word ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Response to Arguments

3. Applicant's arguments with respect to claims 1-30 and 32-34 have been considered but are moot in view of the new ground(s) of rejection due to the newly amended Claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
04/24/06

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER